Memory With 6T Small Aspect Ratio Cells Having Metal_1 Elements Physically Connected to Metal_0 Elements

ABSTRACT OF THE DISCLOSURE

A method of forming memory circuit (20) comprising a plurality of six transistor memory cells (SC_2(WL,C)). The method forms each of the six transistor memory cells to comprise a first inverter having an input and an output and a second inverter having an input and an output. The inverters comprise respective first and second drive transistors (DT1, DT2), each comprising first and second source/drain regions and a gate, and first and second pull-up transistors (PT1, PT2), each comprising first and second source/drain regions and a gate. The output of the first inverter is coupled to the first source/drain region of the first drive transistor and to the first source/drain region of the first pull up transistor. The output of the second inverter is coupled to the first source/drain region of the second drive transistor and to the first source/drain region of the second pull up transistor. Each cell further comprises a first and second access transistor (AT1, AT2), each having a gate, and having a first source/drain region coupled to an inverter output and a second source/drain region for communicating to a corresponding bit line. The method also forms at least one insulating layer (128) in a position relative to the first through sixth transistors, and applies a first mask to the at least one insulating layer to form a plurality of vias through the at least one insulating layer. The method also forms a first conducting layer comprising a plurality of conducting plugs (130_x) in the plurality of vias. The plurality of conducting plugs comprise a first conducting plug (130_4) coupled to the output of the first inverter and a second conducting plug (130_{11}) coupled to the first source/drain region of the first pull-up transistor and to the gate of the second drive transistor and to the gate of the second pull-up transistor. The plurality of conducting plugs further comprise a third conducting plug (130_5) coupled to the output of the second inverter and a fourth conducting plug (130_{12}) coupled to the first source/drain region of the second pull-up transistor and to the gate of the first drive transistor and to the gate of the first pull-up transistor. The method also forms a second conducting layer comprising a plurality of conducting elements (132_x). The plurality of conducting elements comprise a first

conducting element (132_9) coupled to and physically contacting the first conducting plug and coupled to and physically contacting the second conducting plug and a second conducting element (132_{10}) coupled to and physically contacting the third conducting plug and coupled to and physically contacting the fourth conducting plug.